Data Sheet Digest

Sourced May 1, 2023

maxim integrated™

DS1307

64 x 8, Serial, I²C Real-Time Clock

Digital Sundial

DS = ~~Dallas Semiconductor~~

Rev 3/15

Thanks for Listening

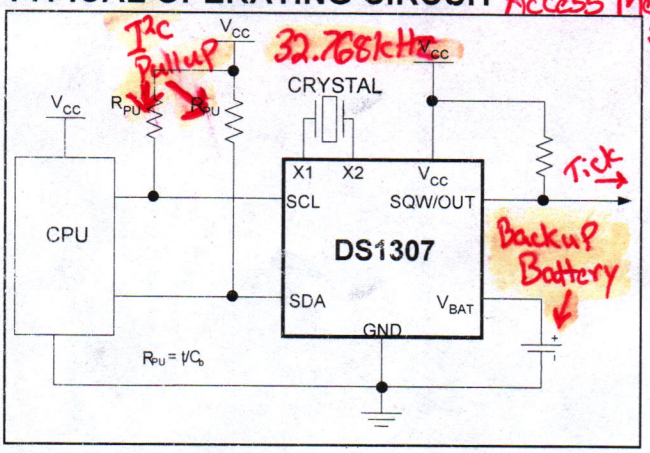
If the year is divisable by 100, but not 400 than the leap year is skipped 2100 doesn't have a leap day

GENERAL DESCRIPTION

The DS1307 serial real-time clock (RTC) is a low-power, full binary-coded decimal (BCD) clock/calendar plus 56 bytes of NV SRAM. Address and data are transferred serially through an I²C, bidirectional bus. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The end of the month date is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator. The DS1307 has a built-in power-sense circuit that detects power failures and automatically switches to the backup supply. Timekeeping operation continues while the part operates from the backup supply.

NVSRAM = Non-Volatile Static Random Access Memory (Battery Backup) Save Games

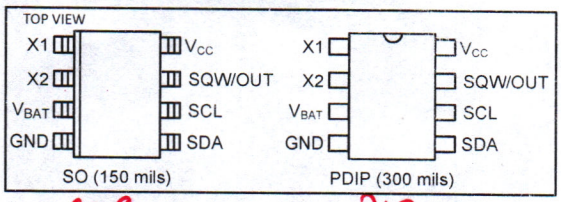
TYPICAL OPERATING CIRCUIT



BENEFITS AND FEATURES

- Completely Manages All Timekeeping Functions
  - Real-Time Clock Counts Seconds, Minutes, Hours, Date of the Month, Month, Day of the Week, and Year with Leap-Year Compensation Valid Up to 2100
  - 56-Byte, Battery-Backed, General-Purpose RAM with Unlimited Writes
  - Programmable Square-Wave Output Signal
- Simple Serial Port Interfaces to Most Microcontrollers (See Page 9)
  - I²C Serial Interface
- Low Power Operation Extends Battery Backup Run Time (0.000,0005 A) (0.5uA)
  - Consumes Less than 500nA in Battery-Backup Mode with Oscillator Running
  - Automatic Power-Fail Detect and Switch Circuitry
- 8-Pin DIP and 8-Pin SO Minimizes Required Space
- Optional Industrial Temperature Range: -40°C to +85°C Supports Operation in a Wide Range of Applications
- Underwriters Laboratories® (UL) Recognized

PIN CONFIGURATIONS



SO-8 DIP

ORDERING INFORMATION

	PART	TEMP RANGE	VOLTAGE (V)	PIN-PACKAGE	TOP MARK*
1	DS1307+	0°C to +70°C	5.0	8 PDIP (300 mils) Tube	DS1307
2	DS1307N+	-40°C to +85°C	5.0	8 PDIP (300 mils) Tube	DS1307N
3	DS1307Z+	0°C to +70°C	5.0	8 SO (150 mils) Tube	DS1307
4	DS1307ZN+	-40°C to +85°C	5.0	8 SO (150 mils) Tube	DS1307N
5	DS1307Z+T&R	0°C to +70°C	5.0	8 SO (150 mils) Tape and Reel	DS1307
6	DS1307ZN+T&R	-40°C to +85°C	5.0	8 SO (150 mils) Tape and Reel	DS1307N

+Denotes a lead-free/RoHS-compliant package.

**A "+" anywhere on the top mark indicates a lead-free package. An "N" anywhere on the top mark indicates an industrial temperature range device.*

Underwriters Laboratories, Inc. is a registered certification mark of Underwriters Laboratories, Inc.

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground ..... -0.5V to +7.0V
-0.5V may damage, but won't function
Operating Temperature Range (Noncondensing)
Commercial ..... 0°C to +70°C
Industrial ..... -40°C to +85°C
Storage Temperature Range ..... -55°C to +125°C
Soldering Temperature (DIP, leads) ..... +260°C for 10 seconds
Soldering Temperature (surface mount) ..... Refer to the JPC/JEDEC J-STD-020 Specification.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0°C to +70°C, T_A = -40°C to +85°C.) (Notes 1, 2)

See notes on Page 6

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
Logic 1 Input	V_{IH}		2.2		V_{CC} + 0.3	V
Logic 0 Input	V_{IL}		-0.3		+0.8	V
V_{BAT} Battery Voltage	V_{BAT}		2.0	3	3.5	V

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V; T_A = 0°C to +70°C, T_A = -40°C to +85°C.) (Notes 1, 2)

Low - 0V - 0.8V
High - 2.2V - Vcc

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage (SCL)	I_{LI}		-1		1	µA
I/O Leakage (SDA, SQW/OUT)	I_{LO}		-1		1	µA
Logic 0 Output (I_{OL} = 5mA)	V_{OL}				0.4	V
Active Supply Current (f_{SCL} = 100kHz)	I_{CCA}				1.5	mA
Standby Current	I_{CCS}	(Note 3)			200	µA
V_{BAT} Leakage Current	I_{BATLKG}			5	50	nA
Power-Fail Voltage (V_{BAT} = 3.0V)	V_{PF}		1.216 x V_{BAT}	1.25 x V_{BAT}	1.284 x V_{BAT}	V

Batt Typ - 3V = 3.65V
Batt Min - 2V = 2.52V

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 0V, V_{BAT} = 3.0V; T_A = 0°C to +70°C, T_A = -40°C to +85°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{BAT} Current (OSC ON); SQW/OUT OFF	I_{BAT1}		0.30uA	300	500	nA
V_{BAT} Current (OSC ON); SQW/OUT ON (32kHz)	I_{BAT2}		0.48uA	480	800	nA
V_{BAT} Data-Retention Current (Oscillator Off)	I_{BATDR}		0.01uA	10	100	nA

3.75V 3.85V
2.5V 2.6V

WARNING: Negative undershoots below -0.3V while the part is in battery-backed mode may cause loss of data.

2

AC ELECTRICAL CHARACTERISTICS

(V$_{CC}$ = 4.5V to 5.5V; T$_A$ = 0°C to +70°C, T$_A$ = -40°C to +85°C.)

The AC characteristics cover data communication, as that is the only alternating current on device.

I²C PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}		0		100	kHz
Bus Free Time Between a STOP and START Condition	t_{BUF}		4.7			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$	(Note 4)	4.0			µs
LOW Period of SCL Clock	t_{LOW}		4.7µs Low clock			µs
HIGH Period of SCL Clock	t_{HIGH}		4.0µs High Clock			µs
Setup Time for a Repeated START Condition	$t_{SU:STA}$		4.7			µs
Data Hold Time	$t_{HD:DAT}$		0			µs
Data Setup Time	$t_{SU:DAT}$	(Notes 5, 6)	250 ns or 0.00025 ms			ns
Rise Time of Both SDA and SCL Signals	t_R				1000	ns
Fall Time of Both SDA and SCL Signals	t_F				300	ns
Setup Time for STOP Condition	$t_{SU:STO}$		4.7			µs

4 MHz ↑ Non-issue?

CAPACITANCE

(T$_A$ = +25°C)

↑ This doesn't include load capacitance on the X1 & X2 pins. For that see page 7.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Pin Capacitance (SDA, SCL)	$C_{I/O}$				10	pF
Capacitance Load for Each Bus Line	C_B	(Note 7)			400	pF

Note 1: All voltages are referenced to ground.

Note 2: Limits at -40°C are guaranteed by design and are not production tested.

Note 3: I_{CCS} specified with V_{CC} = 5.0V and SDA, SCL = 5.0V.

Note 4: After this period, the first clock pulse is generated.

Note 5: A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the $V_{IH(MIN)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Note 6: The maximum $t_{HD:DAT}$ only has to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

Note 7: C_B—total capacitance of one bus line in pF.

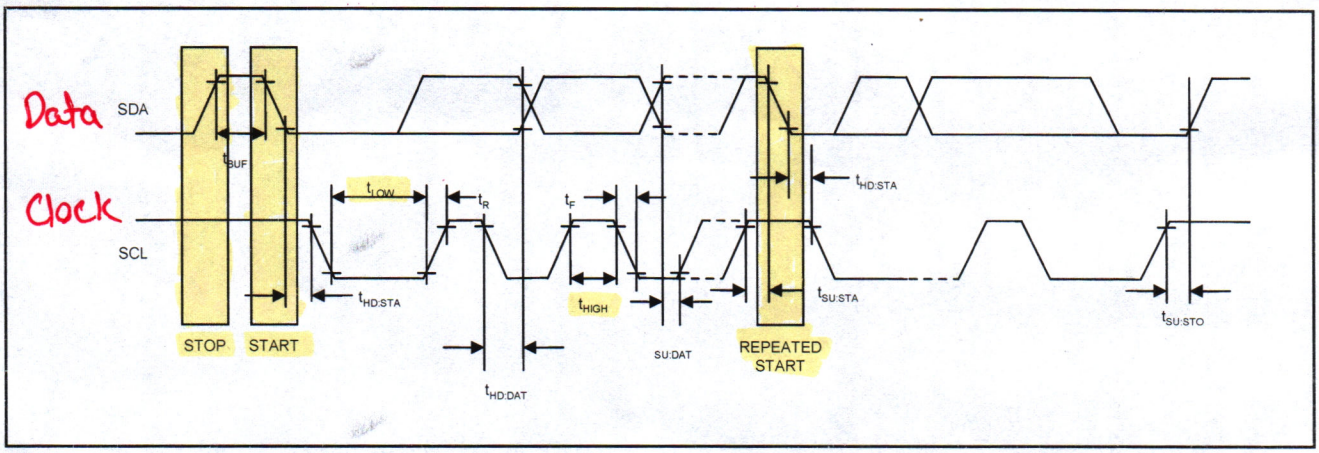
What does the clock signal look like?

Low Period: ≥4.7uS
High Period: ≥4.0uS
Rise Time: <1uS
Fall Time: <300ns

10uS
100kHz? See page 10

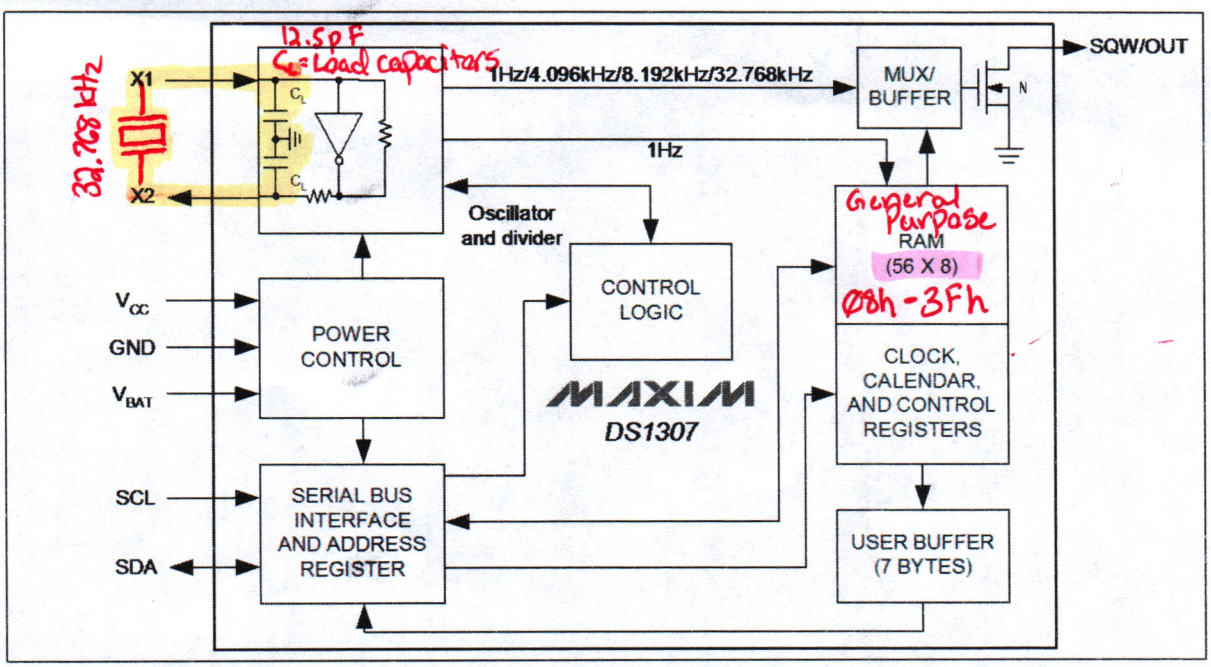
3

TIMING DIAGRAM



See the built in Load Capacitors!

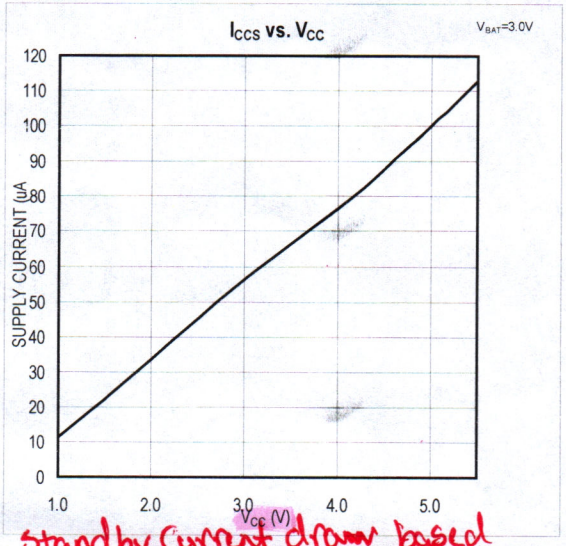
Figure 1. Block Diagram



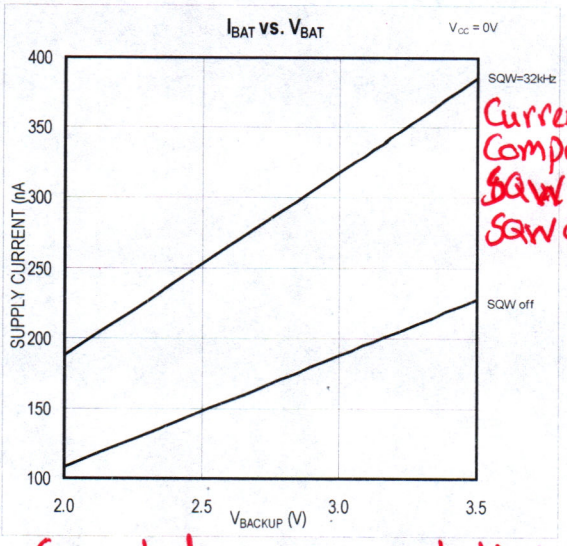
4

TYPICAL OPERATING CHARACTERISTICS

(V_{CC} = 5.0V, T_A = +25°C, unless otherwise noted.)

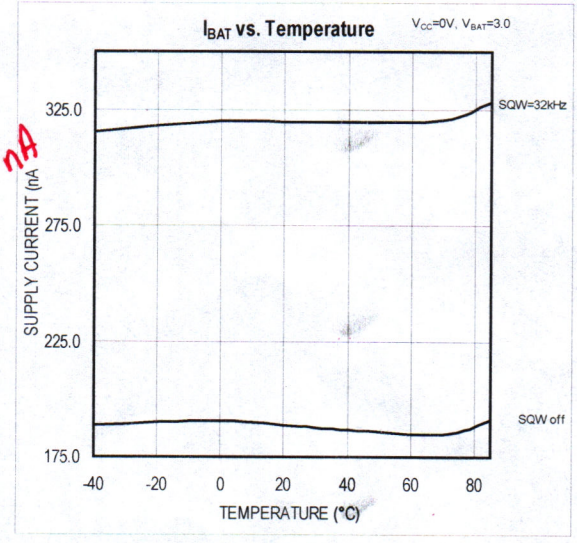


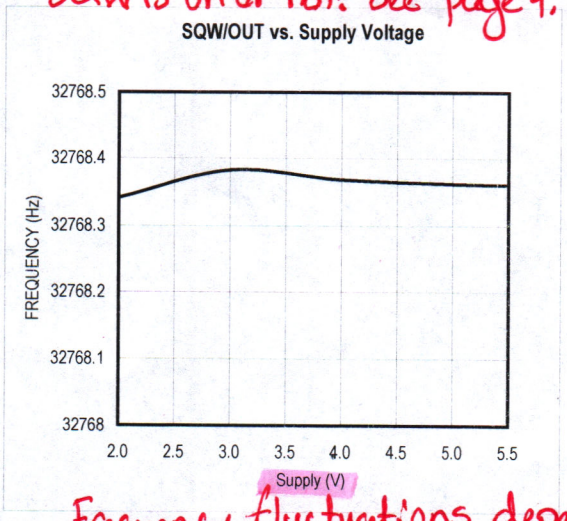
Standby Current draw based on Supply Voltage



Current draw Compared between SQW 32kHz and SQW off.

Current draw when on battery backup power, based on if SQW is on or not. See page 9.





Frequency fluctuations dependant on the Supply Voltage.

? Is Supply(V) different than Vcc(V)?

5

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	X1	Connections for Standard 32.768kHz Quartz Crystal. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (C_L) of 12.5pF. X1 is the input to the oscillator and can optionally be connected to an external 32.768kHz oscillator. The output of the internal oscillator, X2, is floated if an external oscillator is connected to X1. See Page 7 **Note:** For more information on crystal selection and crystal layout considerations, refer to *Application Note 58: Crystal Considerations with Dallas Real-Time Clocks*.
2	X2	
3	V_{BAT}	Backup Supply Input for Any Standard 3V Lithium Cell or Other Energy Source. Battery voltage must be held between the minimum and maximum limits for proper operation. Diodes in series between the battery and the V_{BAT} pin may prevent proper operation. If a backup supply is not required, V_{BAT} must be grounded. The nominal power-fail trip point (V_{PF}) voltage at which access to the RTC and user RAM is denied is set by the internal circuitry as 1.25 x V_{BAT} nominal. A lithium battery with 48mAh or greater will back up the DS1307 for more than 10 years in the absence of power at +25°C. >48 mAh = >10 years UL recognized to ensure against reverse charging current when used with a lithium battery. Go to: www.maxim-ic.com/qa/info/ul/.
4	GND	Ground
5	SDA	Serial Data Input/Output. SDA is the data input/output for the I²C serial interface. The SDA pin is open drain and requires an external pullup resistor. The pullup voltage can be up to 5.5V regardless of the voltage on V_{CC}.
6	SCL	Serial Clock Input. SCL is the clock input for the I²C interface and is used to synchronize data movement on the serial interface. The pullup voltage can be up to 5.5V regardless of the voltage on V_{CC}.
7	SQW/OUT	Square Wave/Output Driver. When enabled, the SQWE bit set to 1, the SQW/OUT pin outputs one of four square-wave frequencies (1Hz, 4kHz, 8kHz, 32kHz). The SQW/OUT pin is open drain and requires an external pullup resistor. SQW/OUT operates with either V_{CC} or V_{BAT} applied. The pullup voltage can be up to 5.5V regardless of the voltage on V_{CC}. If not used, this pin can be left floating.
8	V_{CC}	Primary Power Supply. When voltage is applied within normal limits, the device is fully accessible and data can be written and read. When a backup supply is connected to the device and V_{CC} is below V_{TP}, read and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage.

2.0V - 3.5V

Wow! 2 AA Batteries in series provides 3.1V & 2850 mAh or up to 5990 years... but no writing data

I²C SDA Data

I²C SCL Clock

I²C See Page 10 for more

DETAILED DESCRIPTION

The DS1307 is a low-power clock/calendar with 56 bytes of battery-backed SRAM. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The DS1307 operates as a slave device on the I²C bus. Access is obtained by implementing a START condition and providing a device identification code followed by a register address. Subsequent registers can be accessed sequentially until a STOP condition is executed. When V_{CC} falls below 1.25 x V_{BAT}, the device terminates an access in progress and resets the device address counter. Inputs to the device will not be recognized at this time to prevent erroneous data from being written to the device from an out-of-tolerance system. When V_{CC} falls below V_{BAT}, the device switches into a low-current battery-backup mode. Upon power-up, the device switches from battery to V_{CC} when V_{CC} is greater than V_{BAT} +0.2V and recognizes inputs when V_{CC} is greater than 1.25 x V_{BAT}. The block diagram in Figure 1 shows the main elements of the serial RTC.

Device switches from Battery Backup when Vcc is 1) > VBat + 0.2V and 2) > VBat • 1.25

While in Battery Backup mode, read & write is disabled, but it still keeps time.

If battery isn't required then the VBatt Pin must be grounded. ↳ See Page 2...

On Page 2 it says recomended operating voltage is 4.5V-5.5V, but if VBatt is 3V then 3V • 1.25 is 3.75V.

6

OSCILLATOR CIRCUIT

The DS1307 uses an external 32.768kHz crystal. The oscillator circuit does not require any external resistors or capacitors to operate. Table 1 specifies several crystal parameters for the external crystal. Figure 1 shows a functional schematic of the oscillator circuit. If using a crystal with the specified characteristics, the startup time is usually less than one second.

CLOCK ACCURACY

The accuracy of the clock is dependent upon the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Additional error will be added by crystal frequency drift caused by temperature shifts. External circuit noise coupled into the oscillator circuit may result in the clock running fast. Refer to Application Note 58: *Crystal Considerations with Dallas Real-Time Clocks* for detailed information.

Temp. Compensation based on Crystal performance.

Table 1. Crystal Specifications*

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Nominal Frequency	f_O		32.768		kHz
Series Resistance	ESR			45	kΩ
Load Capacitance	C_L		12.5		pF

**The crystal, traces, and crystal input pins should be isolated from RF generating signals. Refer to Application Note 58: Crystal Considerations for Dallas Real-Time Clocks for additional specifications.*

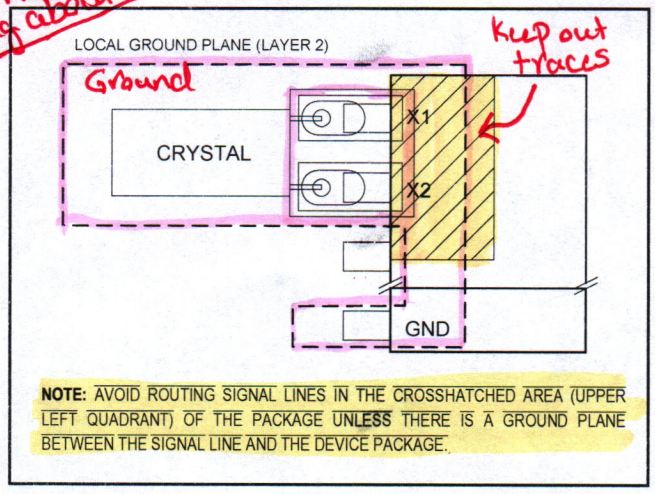
ESR is the Equivalent Series Resistance. When the reactive components of the crystal resonate at the operating frequency. Low ESR = Better

If you're visiting from Page 3 & I was talking about.

See Page 4

All Dallas RTCs have integrated load capacitors. Minimize stray capacitance by keeping the traces short. Traces = small Antennas

Figure 2. Recommended Layout for Crystal



Very interesting. See how the pads for X_1 & X_2 are connected short trace to the Crystal and there is a local Ground fill zone underneath the Crystal.

Table 2 of App Note 58 has a ~~list~~ List of Suitable Crystals

RTC AND RAM ADDRESS MAP

Table 2 shows the address map for the DS1307 RTC and RAM registers. The RTC registers are located in address locations 00h to 07h. The RAM registers are located in address locations 08h to 3Fh. During a multibyte access, when the address pointer reaches 3Fh, the end of RAM space, it wraps around to location 00h, the beginning of the clock space.

Important: If you have a data overflow past 3Fh, the address will advance into the RTC registers. (00h-07h) It is doubly important to never exceed 3Fh. You best write a feature in your software that will forbid going above 3Fh on accident.

7

CLOCK AND CALENDAR

The time and calendar information is obtained by reading the appropriate register bytes. Table 2 shows the RTC registers. The time and calendar are set or initialized by writing the appropriate register bytes. The contents of the time and calendar registers are in the BCD format. The day-of-week register increments at midnight. Values that correspond to the day of week are user-defined but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on.) Illogical time and date entries result in undefined operation. Bit 7 of Register 0 is the clock halt (CH) bit. When this bit is set to 1, the oscillator is disabled. When cleared to 0, the oscillator is enabled. On first application of power to the device the time and date registers are typically reset to 01/01/00 01 00:00:00 (MM/DD/YY DOW HH:MM:SS). The CH bit in the seconds register will be set to a 1. The clock can be halted whenever the timekeeping functions are not required, which minimizes current (I_{BATDR}).

02h

The DS1307 can be run in either 12-hour or 24-hour mode. Bit 6 of the hours register is defined as the 12-hour or 24-hour mode-select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20 to 23 hours). The hours value must be re-entered whenever the 12/24-hour mode bit is changed.

When reading or writing the time and date registers, secondary (user) buffers are used to prevent errors when the internal registers update. When reading the time and date registers, the user buffers are synchronized to the internal registers on any I²C START. The time information is read from these secondary registers while the clock continues to run. This eliminates the need to re-read the registers in case the internal registers update during a read. The divider chain is reset whenever the seconds register is written. Write transfers occur on the I²C acknowledge from the DS1307. Once the divider chain is reset, to avoid rollover issues, the remaining time and date registers must be written within one second.

Table 2. Timekeeper Registers

Nice.

seconds
minutes
hours
Day
Date
Month
Year
control

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION	RANGE
00h	CH	10 Seconds			Seconds				Seconds	00–59
01h	0	10 Minutes			Minutes				Minutes	00–59
02h	0	12/24 (High select 12/24 bit)	10 Hour / PM/AM	10 Hour	Hours				Hours	1–12 +AM/PM 00–23
03h	0	0	0	0	0	DAY			Day	01–07
04h	0	0	10 Date		Date				Date	01–31
05h	0	0	0	10 Month	Month				Month	01–12
06h	10 Year				Year				Year	00–99
07h	OUT	0	0	SQWE	0	0	RS1	RS0	Control	—
08h–3Fh	56 Bytes of NVSRAM for Activities								RAM 56 x 8	00h–FFh

0 = Always reads back as 0.

CH = Clock Halt = when 1-osc disabled = 0.01uA = keeps track of time when stopped

↑

10nA - No practical Current

8

CONTROL REGISTER

The DS1307 control register is used to control the operation of the SQW/OUT pin. 07h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
OUT	0	0	SQWE	0	0	RS1	RS0

Bit 7: Output Control (OUT). This bit controls the output level of the SQW/OUT pin when the square-wave output is disabled. If SQWE = 0, the logic level on the SQW/OUT pin is 1 if OUT = 1 and is 0 if OUT = 0. On initial application of power to the device, this bit is typically set to a 0. When SQWE is 0 & OUT is 1, then the output pin is a constant high

Bit 4: Square-Wave Enable (SQWE). This bit, when set to logic 1, enables the oscillator output. The frequency of the square-wave output depends upon the value of the RS0 and RS1 bits. With the square-wave output set to 1Hz, the clock registers update on the falling edge of the square wave. On initial application of power to the device, this bit is typically set to a 0. This bit has an impact on Power Consumption

Bits 1 and 0: Rate Select (RS[1:0]). These bits control the frequency of the square-wave output when the square-wave output has been enabled. The following table lists the square-wave frequencies that can be selected with the RS bits. On initial application of power to the device, these bits are typically set to a 1.

RS1	RS0	SQW/OUT OUTPUT	SQWE	OUT
0	0	1Hz	1	X
0	1	4.096kHz	1	X
1	0	8.192kHz	1	X
1	1	32.768kHz	1	X
X	X	0 Off	0	0
X	X	1 Always On	0	1

Square Wave out Control makes Output pin Constantly a logic high when the oscillator is disabled.

9

I²C DATA BUS

See also Page 3.

The DS1307 supports the I²C protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are referred to as slaves. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The DS1307 operates as a slave on the I²C bus.

Figures 3, 4, and 5 detail how data is transferred on the I²C bus.

Buckle up, now is time for a Crash Course in I²C data Communication

- Data transfer can be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is high will be interpreted as control signals.

Not Busy Clock High Data High
Start Change H→L High
Stop L→H High

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

START data transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

STOP data transfer: A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Control Signals

Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited, and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit. Within the I²C bus specifications a standard mode (100kHz clock rate) and a fast mode (400kHz clock rate) are defined. The DS1307 operates in the standard mode (100kHz) only.

Clock Speed: 100kHz

yep

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

For each byte, except last

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

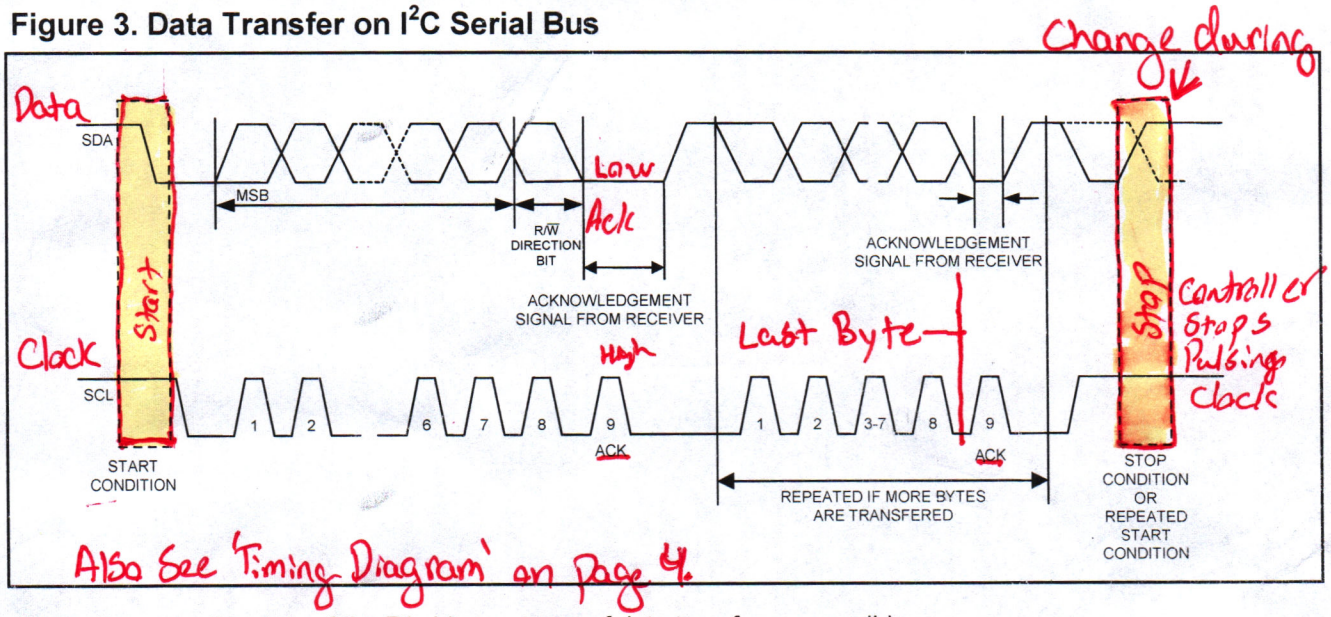
[redacted]

Data holds high at every clock pulse. This means 'Not Busy'. When data goes Low DURING the Clock Pulse. It Signifies the Start of Communication

	Clock	Data
Not Busy	High	High
Start	High	High to Low Change
Stop	High	Low to High Change
Acknowledge	High	Low

10

Figure 3. Data Transfer on I²C Serial Bus



Also See 'Timing Diagram' on Page 4.

Depending upon the state of the R/W bit, two types of data transfer are possible:

1. **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first.

2. **Data transfer from a slave transmitter to a master receiver.** The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. This is followed by the slave transmitting a number of data bytes. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a "not acknowledge" is returned.

The master device generates all the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released. Data is transferred with the most significant bit (MSB) first.

Clock Pulses are generated by the Controller and read by the I²C Device.
Start & Stop are generated by Controller
Acknowledge is sent from the receiver
Data is always sent with the MSB first

11

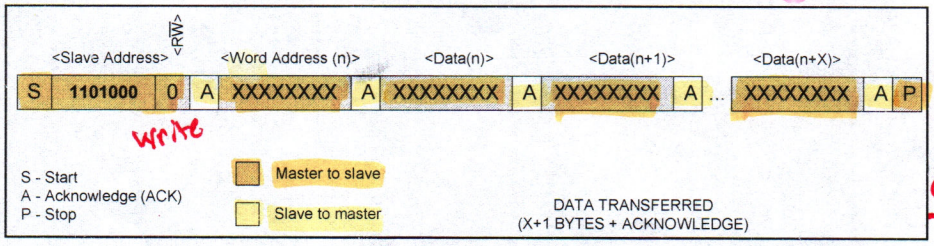
The DS1307 can operate in the following two modes:

1. **Slave Receiver Mode (Write Mode):** Serial data and clock are received through SDA and SCL. After each byte is received an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Hardware performs address recognition after reception of the slave address and direction bit (see Figure 4). The slave address byte is the first byte received after the master generates the START condition. The slave address byte contains the 7-bit DS1307 address, which is 1101000, followed by the direction bit (R/$\overline{W}$), which for a write is 0. After receiving and decoding the slave address byte, the DS1307 outputs an acknowledge on SDA. After the DS1307 acknowledges the slave address + write bit, the master transmits a word address to the DS1307. This sets the register pointer on the DS1307, with the DS1307 acknowledging the transfer. The master can then transmit zero or more bytes of data with the DS1307 acknowledging each byte received. The register pointer automatically increments after each data byte are written. The master will generate a STOP condition to terminate the data write.

2. **Slave Transmitter Mode (Read Mode):** The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit will indicate that the transfer direction is reversed. The DS1307 transmits serial data on SDA while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer (see Figure 5). The slave address byte is the first byte received after the START condition is generated by the master. The slave address byte contains the 7-bit DS1307 address, which is 1101000, followed by the direction bit (R/$\overline{W}$), which is 1 for a read. After receiving and decoding the slave address the DS1307 outputs an acknowledge on SDA. The DS1307 then begins to transmit data starting with the register address pointed to by the register pointer. If the register pointer is not written to before the initiation of a read mode the first address that is read is the last one stored in the register pointer. The register pointer automatically increments after each byte are read. The DS1307 must receive a Not Acknowledge to end a read.

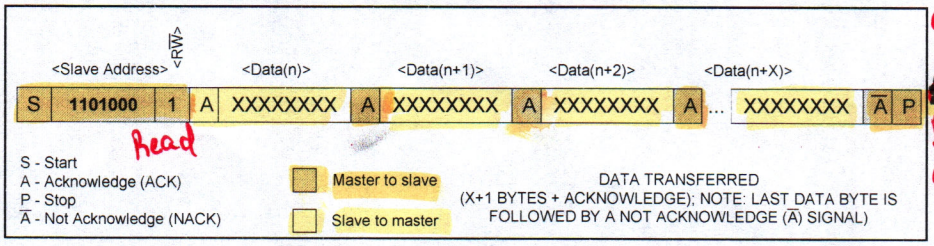
White Write: bit Ø, Byte Ø = Ø → Address byte — 1bit
Read: bit Ø, Byte Ø = 1 → 7bit

Figure 4. Data Write—Slave Receiver Mode



Controller: Start → address → write
Device: Ack
Controller: 1 Byte of data
Device: Ack
... and so on ...
Controller: Stop

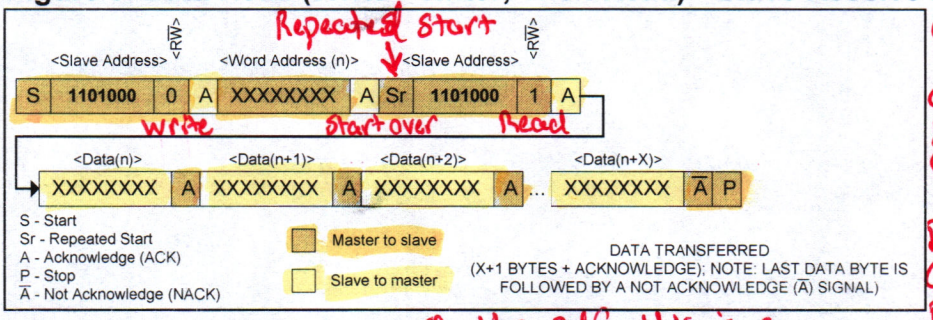
Figure 5. Data Read—Slave Transmitter Mode



7-bit 1-bit
Controller: Start → address → Read
Device: Ack → 1Byte of data
[redacted] Controller: Ack
Device: 1 Byte of Data
Controller: Ack
... Until all requested data is received...
Controller: [redacted] Not Ack + Stop

12

Figure 6. Data Read (Write Pointer, Then Read)—Slave Receive and Transmit



7-bit 1-bit
Controller: Start + address → write
Device: Ack
Controller: Start at this register
Device: Ack
Controller: Nevermind address
We're going to start reading
Device: Ack → 1 Byte of data
Controller: Ack
Device: 1- Byte of data.
Controller: Ack

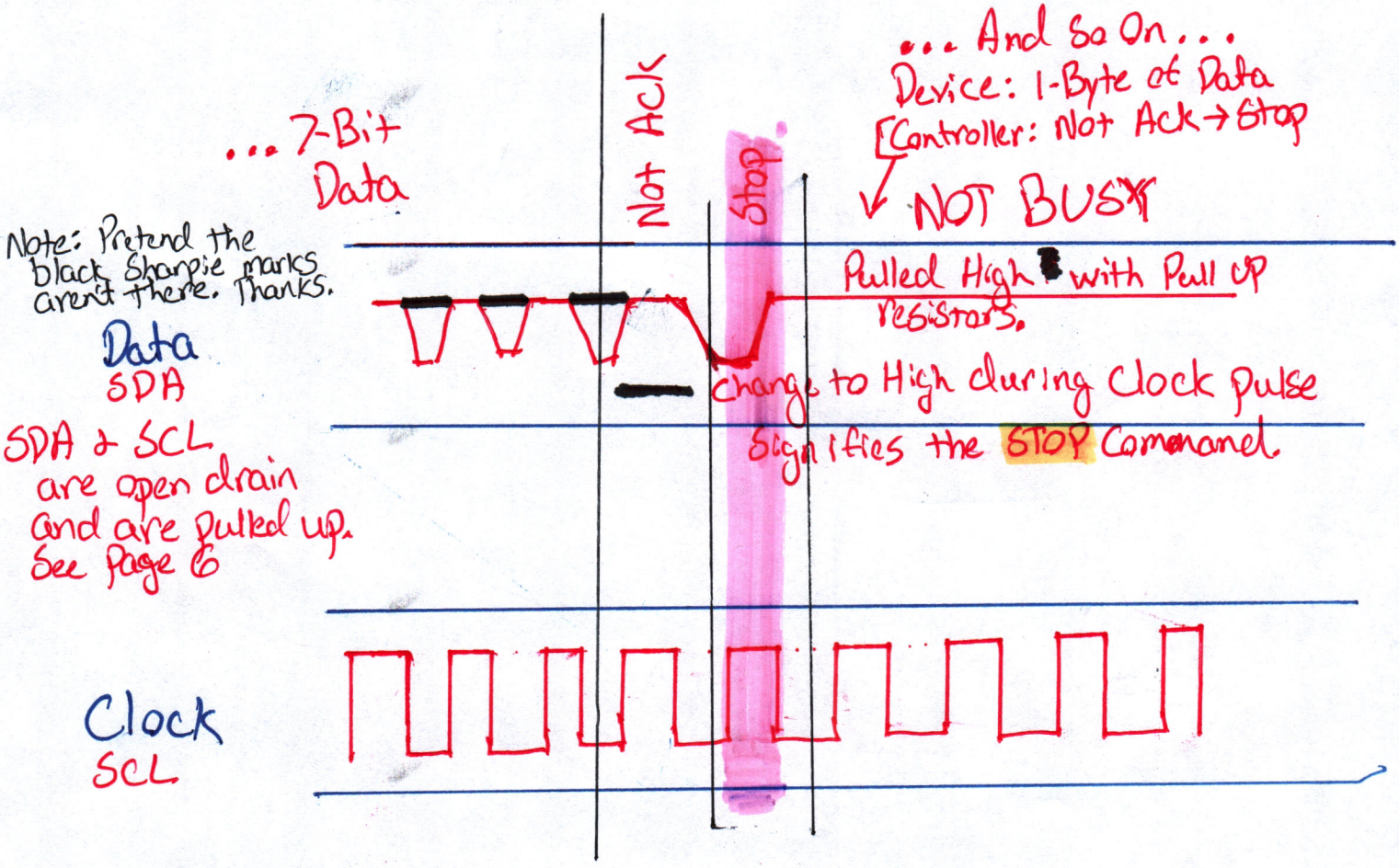
On the pdf this is a Hyperlinks

PACKAGE INFORMATION

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
8 PDIP THT	—	21-0043
8 SO SMT	—	21-0041

... And So On...
Device: 1-Byte of Data
Controller: Not Ack → Stop
NOT BUSY



13

REVISION HISTORY ← WOW!

REVISION DATE	DESCRIPTION	PAGES CHANGED
1 100208	Moved the *Typical Operating Circuit* and *Pin Configurations* to first page.	1
	Removed the leaded part numbers from the *Ordering Information* table.	1
	Added an open-drain transistor to SQW/OUT in the block diagram (Figure 1).	4
	Added the pullup voltage range for SDA, SCL, and SQW/OUT to the *Pin Description* table and noted that SQW/OUT can be left open if not used.	6
	Added default time and date values on first application of power to the *Clock and Calendar* section and deleted the note that initial power-on state is not defined.	8
	Added default on initial application of power to bit info in the *Control Register* section.	9
	Updated the *Package Information* section to reflect new package outline drawing numbers.	13
2 3/15	Updated *Benefits and Features* section	1

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600

14

Datasheet Evaluation and Analysis Report

Part Number:	DS B07	**Manufacturer:**	Maxim → Analog Devices
Datasheet Revision:	3/15	**Date Published:**	3/15
Datasheet Source:	Analog Devices	**Date Sourced:**	1 May 2023
Evaluated By:	David Ray	**Final Score:**	~~348~~ /555 Points
Additional Notes:			341 / 555 points

1. Presentation and Accessibility (75 points)	
- Language (10 points)	8 - English Only Some translations online
- Readability (10 points)	10
- Availability (10 points)	10
- Ease of Access (10 points)	10
- Content-Length Efficiency (5 points)	5
- Mobile Compatibility (5 points)	~~10~~ Hyperlink to Ordering page
- Hyperlinks (10 points)	~~10~~ 0 → No Links to App Note 58 All Links Broken
- Searchability (10 points)	10 - Searchable PDF
- Consistent Formatting (5 points)	5
Score: Section 1 (75 points)	~~68~~ 61
Section Notes:	

2. Organization and Layout (60 points)	
- Table of Contents and Navigation (10 points)	0
- Clarity of Information (10 points)	10
- Use of Graphics (10 points)	10
- Data Sheet Structure (10 points)	10
- Consistent Terminology (10 points)	10
- Section Headings (5 points)	5
- Subsection Headings (5 points)	5
Score: Section 2 (60 points)	50
Section Notes:	

3. Electrical Characteristics (90 points)	
- Absolute Maximum Ratings (10 points)	10
- Recommended Operating Conditions (10 points)	10
- Electrical Characteristics (10 points)	10
- Dynamic Characteristics (10 points)	10
- Thermal Characteristics (10 points)	6
- Noise Characteristics (10 points)	0
- Power Consumption (10 points)	10
- Accuracy and Precision (10 points)	10
- Output Drive Capability (10 points)	10
Score: Section 3 (90 points)	76

Section Notes:

4. Functional Description (75 points)	
- Pin Configuration (10 points)	10 Page 6
- Pin Functions (10 points)	10
- Function Tables (10 points)	10
- Block Diagram (10 points)	10
- Performance Diagrams (10 points)	10
- Signal Descriptions (10 points)	10
- Input/Output Waveforms (5 points)	5
- Functional Diagrams (5 points)	5
Score: Section 4 (75 points)	75 points!

Section Notes:

Part Number: DS1307

5. Application Information (60 points)	
- Typical Applications (10 points)	0
- Circuit Description (10 points)	10
- PCB Footprint and Layout (10 points)	8 → Hyperlinks on page 13 are dead
- Reference Designs (10 points)	10
- Application Notes (10 points)	10
- Component Selection Guidelines (5 points)	1 → in app note 58 but no Hyperlink
- Power Supply Recommendations (5 points)	3
Score: Section 5 (60 points)	34
Section Notes:	

6. Quality and Reliability (75 points)	
- Quality Standards and Certifications (10 points)	5 UL Recognized
- Reliability Information (10 points)	2 → Battery Data
- Failure Rate Data (10 points)	0
- Test and Evaluation Procedures (10 points)	0
- Environmental Considerations (10 points)	0
- ESD Handling Precautions (10 points)	0
- MTBF Data (5 points)	0
- Burn-in and Screening Procedures (5 points)	0
- Life Cycle Status (5 points)	0
Score: Section 6 (75 points)	7
Section Notes:	

7. Packaging and Handling (30 points)	
- Packaging Information (10 points)	0 → Links on on page 13
- Handling Precautions (10 points)	0 → All Links on Page 13 = Dead
- Storage and Shelf Life (5 points)	0
- Labeling and Marking (5 points)	0
Score: Section 7 (30 points)	0
Section Notes:	

8. Support and Documentation (60 points)	
- Additional Documentation (10 points)	4 Calls for Docs, but links are broken
- Design Resources (10 points)	4 → drawings + Schematics
- Technical Support (10 points)	0
- Community Resources (10 points)	5 → None from OEM Brands
- Errata Sheets (5 points)	0
- Frequently Asked Questions (5 points)	0
- Software Tools and Drivers (5 points)	0
- Application Examples (5 points)	0
Score: Section 8 (60 points)	13
Section Notes:	

9. Updates and Revision Control (30 points)	
- Revision History (15 points)	10 → Incomplete
- Update Frequency (15 points)	0
Score: Section 9 (30 points)	10
Section Notes:	

Datasheet Evaluation and Analysis Report

10. Overall Impression (15 points)	
- Organization and Clarity (5 points)	5
- Completeness of Information (5 points)	5
- Relevance to Application (5 points)	5
Score: Section 10 (15 points)	15
Section Notes:	
Total Score: (555 points)	~~348~~ 341
Summary and Reflection: Great datasheet, but it doesn't seem to have been maintained since Analog Devices acquired Maxim Integrated. It is a Shame	

Part Number: DS 1307